

Sensitive Gate TRIACS

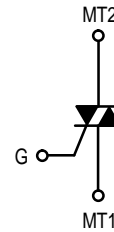
Silicon Bidirectional Thyristors

Designed for high volume, low cost, industrial and consumer applications such as motor control; process control; temperature, light and speed control.

- Small Size Surface Mount DPAK Package
- Passivated Die for Reliability and Uniformity
- Four-Quadrant Triggering
- Blocking Voltage to 600 V
- On-State Current Rating of 4.0 Amperes RMS at 93°C
- Low Level Triggering and Holding Characteristics

ORDERING INFORMATION

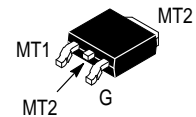
- To Obtain "DPAK" in Surface Mount Leadform (Case 369A)
Shipped in Sleeves — No Suffix, i.e. MAC4DHM
Shipped in 16 mm Tape and Reel — Add "T4" Suffix to Device Number, i.e. MAC4DHMT4
- To Obtain "DPAK" in Straight Lead Version (Case 369) Shipped in Sleeves — Add "-1" Suffix to Device Number, i.e. MAC4DHM-1



MAC4DHM
MAC4DLM

Motorola Preferred Devices

TRIACS
4.0 AMPERES RMS
600 VOLTS



CASE 369A-13
STYLE 6

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Peak Repetitive Off-State Voltage (1) (T _J = -40 to 110°C, Sine Wave, 50 to 60 Hz, Gate Open)	V _{DRM}	600 600	Volts
On-State RMS Current (Full Cycle Sine Wave, 60 Hz, T _C = 93°C)	I _{T(RMS)}	4.0	Amps
Peak Non-Repetitive Surge Current (One Full Cycle, 60 Hz, T _J = 110°C)	I _{TSM}	40	
Circuit Fusing Consideration (t = 8.3 msec)	i ² t	6.6	A ² sec
Peak Gate Power (Pulse Width ≤ 10 μsec, T _C = 93°C)	P _{GM}	0.5	Watts
Average Gate Power (t = 8.3 msec, T _C = 93°C)	P _{G(AV)}	0.1	
Peak Gate Current (Pulse Width ≤ 10 μsec, T _C = 93°C)	I _{GM}	0.2	Amps
Peak Gate Voltage (Pulse Width ≤ 10 μsec, T _C = 93°C)	V _{GM}	5.0	Volts
Operating Junction Temperature Range	T _J	-40 to 110	°C
Storage Temperature Range	T _{stg}	-40 to 150	

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance — Junction to Case	R _{θJC}	3.5	°C/W
— Junction to Ambient	R _{θJA}	88	
— Junction to Ambient (2)	R _{θJA}	80	
Maximum Lead Temperature for Soldering Purposes (3)	T _L	260	°C

(1) V_{DRM} for all types can be applied on a continuous basis. Ratings apply for zero or negative gate voltage; positive gate voltage shall not be applied concurrent with negative potential on the anode. Blocking voltages shall not be tested with a constant current source such that the voltage ratings of the device are exceeded.

(2) Surface mounted on minimum recommended pad size.

(3) 1/8" from case for 10 seconds.

Preferred devices are Motorola recommended choices for future use and best overall value.

MAC4DHM MAC4DLM

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Characteristics	Symbol	Min	Typ	Max	Unit
Peak Repetitive Blocking Current (V _D = Rated V _{DRM} , Gate Open) T _J = 25°C T _J = 110°C	I _{DRM}	— —	— —	0.01 2.0	mA
Peak On-State Voltage (1) (I _{TM} = ±6.0 A)	V _{TM}	—	1.3	1.6	Volts
Gate Trigger Current (Continuous dc) (V _D = 12 V, R _L = 100 Ω) MT2(+), G(+) MAC4DLM MT2(+), G(-) MT2(-), G(-) MT2(-), G(+) MT2(+), G(+) MAC4DHM MT2(+), G(-) MT2(-), G(-) MT2(-), G(+)	I _{GT}	— — — — — — — —	1.8 2.1 2.4 4.2 1.8 2.1 2.4 4.2	3.0 3.0 3.0 5.0 5.0 5.0 5.0 10	mA
Gate Trigger Voltage (Continuous dc) (V _D = 12 V, R _L = 100 Ω) MT2(+), G(+) MT2(+), G(-) MT2(-), G(-) MT2(-), G(+) (V _D = 12 V, R _L = 10 K Ω, T _J = 110°C) MT2(+), G(+); MT2(+), G(-); MT2(-), G(-); MT2(-), G(+)	V _{GT}	0.5 0.5 0.5 0.5 0.1	0.62 0.57 0.65 0.74 0.4	1.3 1.3 1.3 1.3 —	Volts
Holding Current (V _D = 12 V, Gate Open, I _T = ±200 mA)	I _H	—	1.5	15	mA
Latching Current MT2(+), G(+) (V _D = 12 V, I _G = 5.0 mA) MT2(+), G(-) (V _D = 12 V, I _G = 5.0 mA) MT2(-), G(-) (V _D = 12 V, I _G = 5.0 mA) MT2(-), G(+) (V _D = 12 V, I _G = 10 mA)	I _L	— — — —	1.75 5.2 2.1 2.2	10 10 10 10	mA

DYNAMIC CHARACTERISTICS

Characteristics	Symbol	Min	Typ	Max	Unit
Rate of Change of Commutating Current (1) (V _D = 200 V, I _{TM} = 1.8 A, Commutating dv/dt = 1.0 V/μsec, T _J = 110°C, f = 250 Hz, CL = 5.0 μfd, LL = 80 mH, RS = 56 Ω, CS = 0.03 μfd) See Figure 10	di/dt(c)	—	3.0	—	A/ms
Critical Rate of Rise of Off-State Voltage (V _D = 0.67 X Rated V _{DRM} , Exponential Waveform, Gate Open, T _J = 110°C)	dv/dt	—	10	—	V/μs

(1) Pulse test: Pulse Width ≤ 2.0 msec, Duty Cycle ≤ 2%.

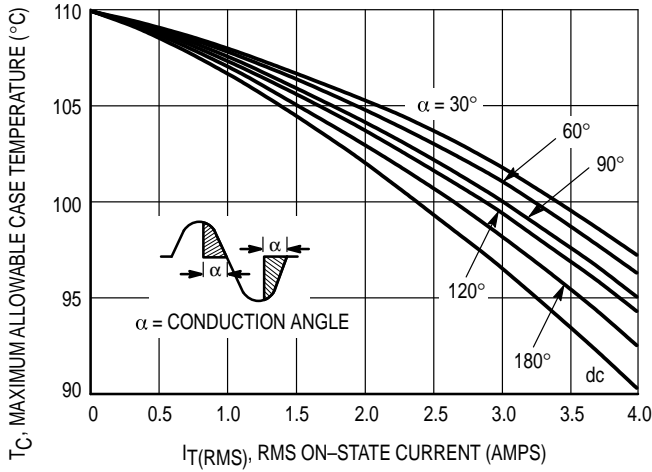


Figure 1. RMS Current Derating

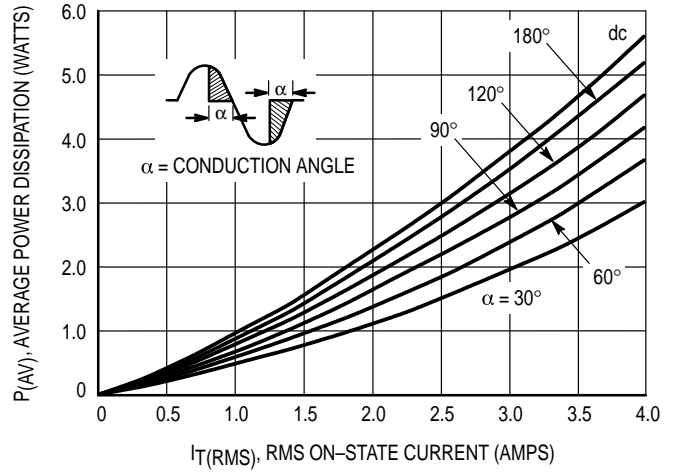


Figure 2. On-State Power Dissipation

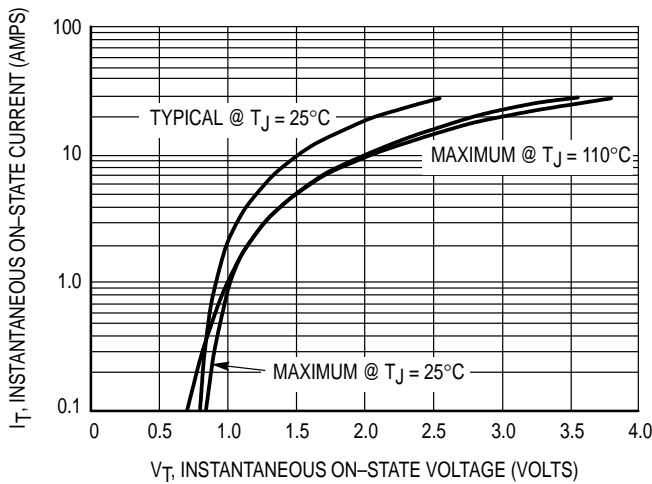


Figure 3. On-State Characteristics

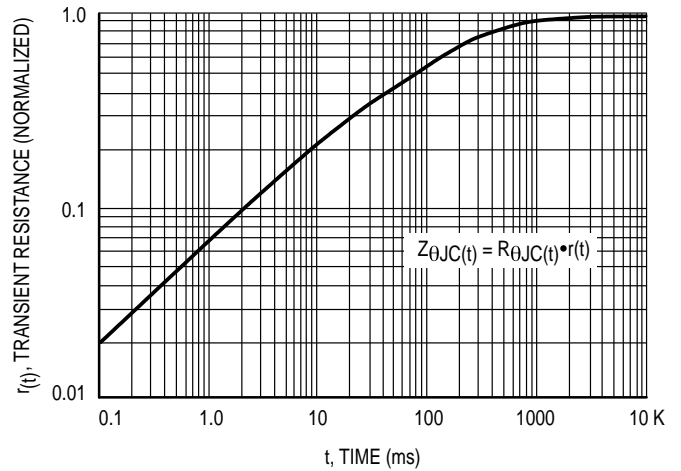


Figure 4. Transient Thermal Response

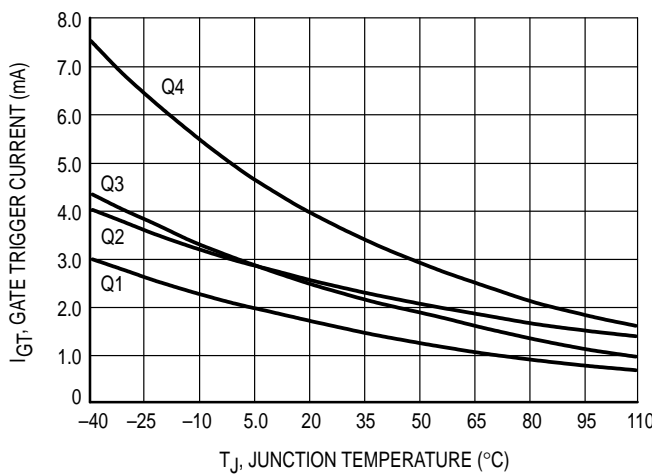


Figure 5. Typical Gate Trigger Current versus Junction Temperature

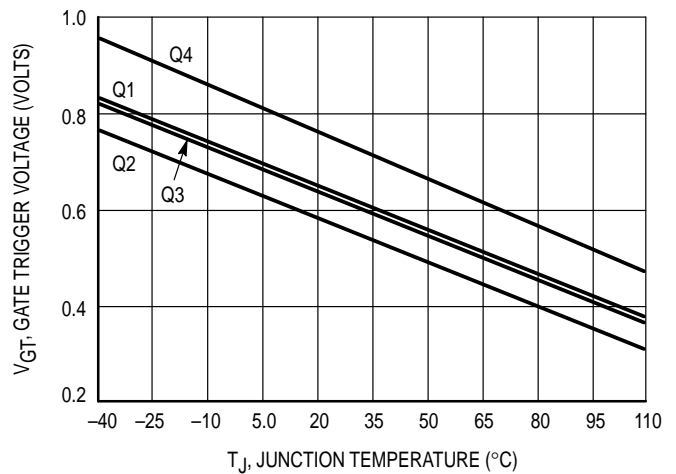


Figure 6. Typical Gate Trigger Voltage versus Junction Temperature

MAC4DHM MAC4DLM

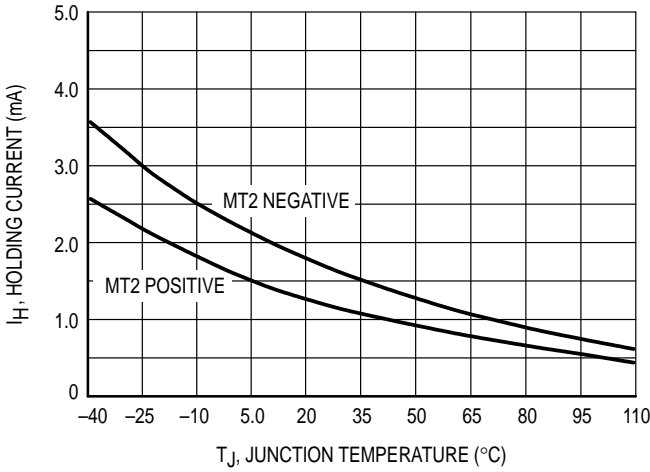


Figure 7. Typical Holding Current versus Junction Temperature

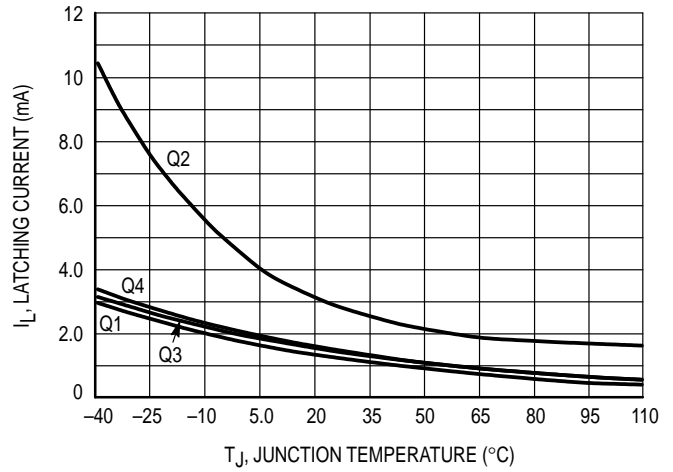


Figure 8. Typical Latching Current versus Junction Temperature

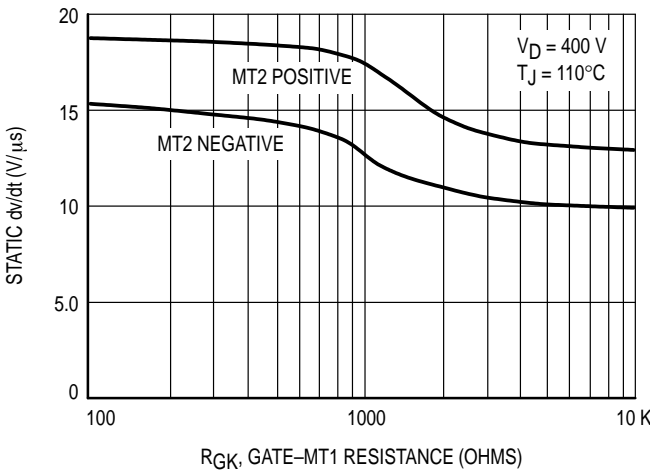


Figure 9. Exponential Static dv/dt versus Gate-MT1 Resistance, MT2(+)

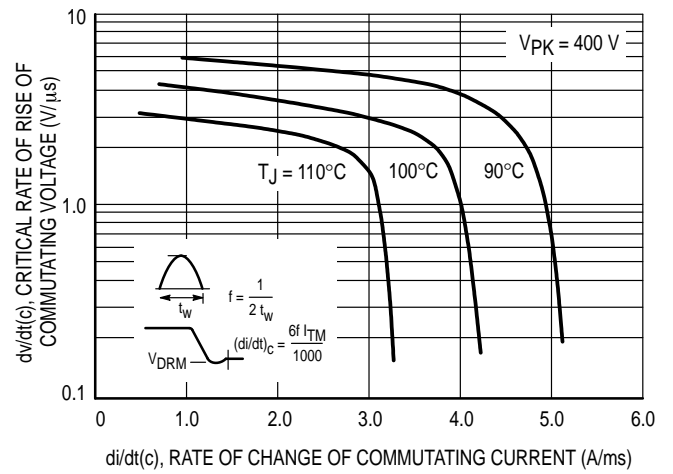
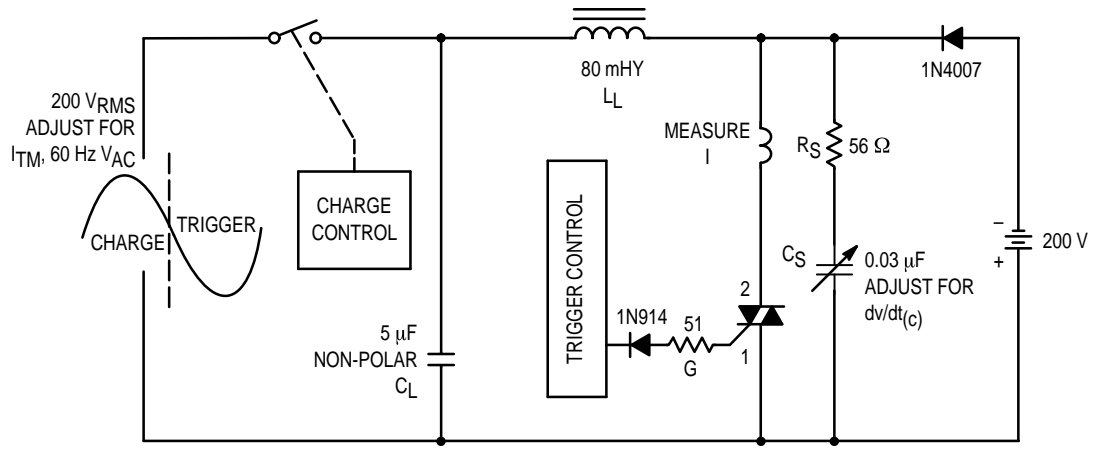


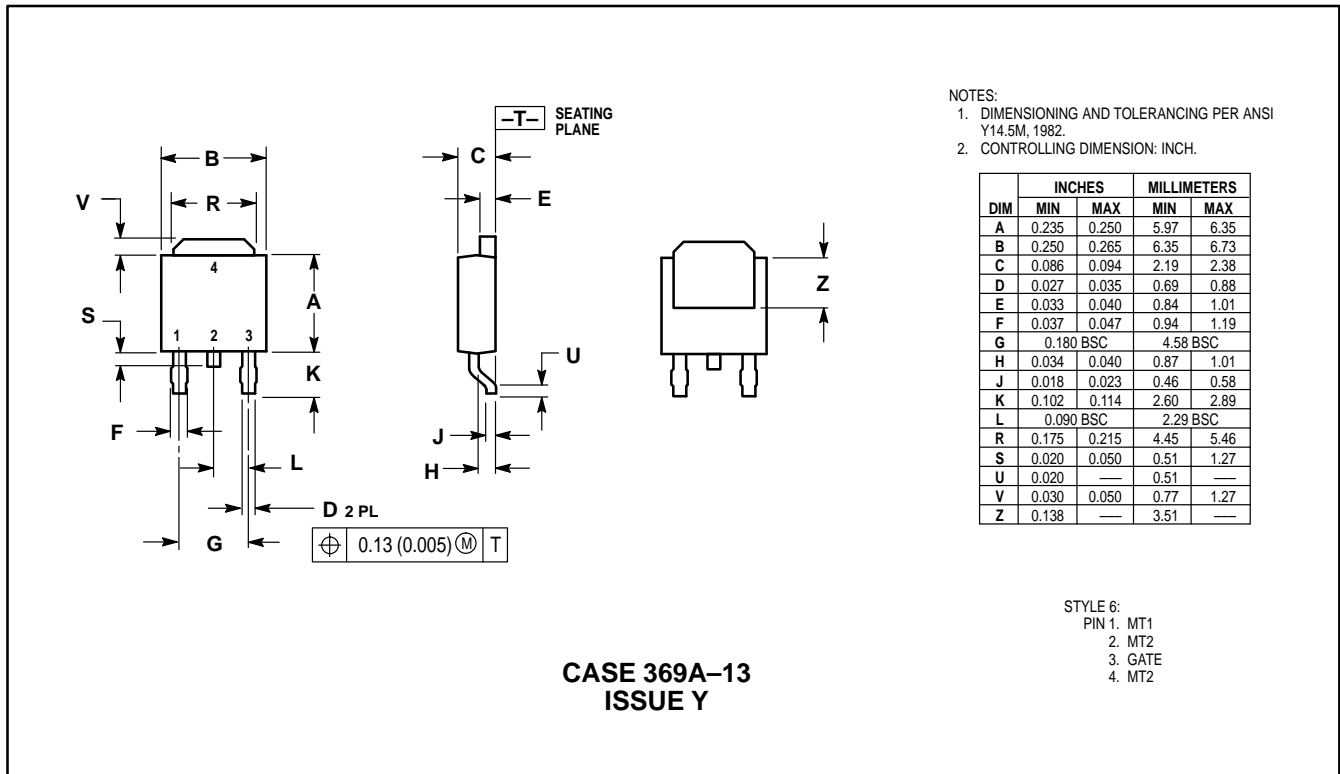
Figure 10. Critical Rate of Rise of Commutating Voltage



Note: Component values are for verification of rated $(dv/dt)_c$. See AN1048 for additional information.

Figure 11. Simplified Test Circuit to Measure the Critical Rate of Rise of Commutating Voltage

PACKAGE DIMENSIONS



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