TRIACS

Silicon Bidirectional Thyristors

Designed for high volume, low cost, industrial and consumer applications such as motor control; process control; temperature, light and speed control.

- Small Size Surface Mount DPAK Package
- · Passivated Die for Reliability and Uniformity
- Blocking Voltage to 800 V
- On-State Current Rating of 4.0 Amperes RMS at 108°C
- Low IGT 10 mA Maximum in 3 Quadrants
- High Immunity to dv/dt 50 V/μs at 125°C

ORDERING INFORMATION

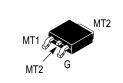
- To Obtain "DPAK" in Surface Mount Leadform (Case 369A)
 Shipped in Sleeves No Suffix, i.e. MAC4DSN
 Shipped in 16 mm Tape and Reel Add "T4" Suffix to Device Number, i.e. MAC4DSNT4
- To Obtain "DPAK" in Straight Lead Version (Case 369) Shipped in Sleeves Add "-1" Suffix to Device Number, i.e. MAC4DSN-1

MAC4DSM MAC4DSN

Motorola Preferred Devices

TRIACS
4.0 AMPERES RMS
600 thru 800 VOLTS

MT2



CASE 369A-13 STYLE 6

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Rating		Symbol	Value	Unit
Peak Repetitive Off–State Voltage ⁽¹⁾ (T _J = -40 to 125°C, Sine Wave, 50 to 60 Hz, Gate Open)	MAC4DSM MAC4DSN	VDRM	600 800	Volts
On–State RMS Current (Full Cycle Sine Wave, 60 Hz, T _C = 108°C)		l _{T(RMS)}	4.0	Amps
Peak Non–Repetitive Surge Current (One Full Cycle, 60 Hz, T _J = 125°C)		ITSM	40	
Circuit Fusing Consideration (t = 8.3 msec)		l ² t	6.6	A ² sec
Peak Gate Power (Pulse Width ≤ 10 μsec, T _C = 108°C)		P _{GM}	0.5	Watts
Average Gate Power (t = 8.3 msec, T _C = 108°C)		P _{G(AV)}	0.1	
Peak Gate Current (Pulse Width ≤ 10 μsec, T _C = 108°C)		I _{GM}	0.2	Amps
Peak Gate Voltage (Pulse Width ≤ 10 μsec, T _C = 108°C)		V _{GM}	5.0	Volts
Operating Junction Temperature Range		TJ	-40 to 125	°C
Storage Temperature Range		T _{stg}	-40 to 150	

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance — Junction to Case — Junction to Ambient — Junction to Ambient (2)	R _θ JC R _θ JA R _θ JA	3.5 88 80	°C/W
Maximum Lead Temperature for Soldering Purposes (3)	TL	260	°C

- (1) V_{DRM} for all types can be applied on a continuous basis. Ratings apply for zero or negative gate voltage; positive gate voltage shall not be applied concurrent with negative potential on the anode. Blocking voltages shall not be tested with a constant current source such that the voltage ratings of the device are exceeded.
- (2) Surface mounted on minimum recommended pad size.
- (3) 1/8" from case for 10 seconds.

Preferred devices are Motorola recommended choices for future use and best overall value.



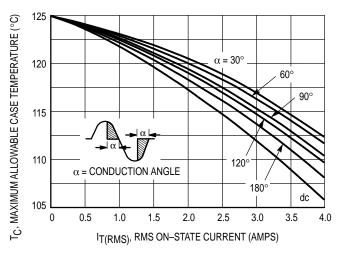
ELECTRICAL CHARACTERISTICS ($T_J = 25$ °C unless otherwise noted)

Characteristics	Symbol	Min	Тур	Max	Unit
Peak Repetitive Blocking Current (V_D = Rated V_{DRM} , Gate Open) $T_J = 25^{\circ}C$ $T_J = 125^{\circ}C$	IDRM	_	=	0.01 2.0	mA
Peak On–State Voltage (1) (I _{TM} = ±6.0 A)	VTM	_	1.3	1.6	Volts
Gate Trigger Current (Continuous dc) (V $_D$ = 12 V, R $_L$ = 100 Ω) MT2(+), G(+) MT2(+), G(-) MT2(-), G(-)	ЧGТ	2.9 2.9 2.9	4.0 5.0 7.0	10 10 10	mA
Gate Trigger Voltage (Continuous dc) (V_D = 12 V, R_L = 100 Ω) MT2(+), G(+) MT2(+), G(-) MT2(-), G(-) MT2(+), G(+); MT2(+), G(-); MT2(-), G(-) T _J = 125°C	Vgт	0.5 0.5 0.5 0.2	0.7 0.65 0.7 0.4	1.3 1.3 1.3 —	Volts
Holding Current (V _D = 12 V, Gate Open, I _T = ±200 mA)	lн	2.0	5.5	15	mA
Latching Current ($V_D = 12 \text{ V}, I_G = 10 \text{ mA}$) MT2(+), G(+) MT2(+), G(-) MT2(-), G(-)	IL.		6.0 10 6.0	30 30 30	mA

DYNAMIC CHARACTERISTICS

Characteristics	Symbol	Min	Тур	Max	Unit
Rate of Change of Commutating Current $^{(1)}$ (V _D = 400 V, I _{TM} = 3.5 A, Commutating dv/dt = 10 V/ μ sec, Gate Open, T _J = 125°C, f = 500 Hz, CL = 5.0 μ F, LL = 20 mH, No Snubber) See Figure 15	di/dt(c)	3.0	4.0		A/ms
Critical Rate of Rise of Off–State Voltage (V _D = 0.67 X Rated V _{DRM} , Exponential Waveform, Gate Open, T _J = 125°C)	dv/dt	50	175	_	V/μs

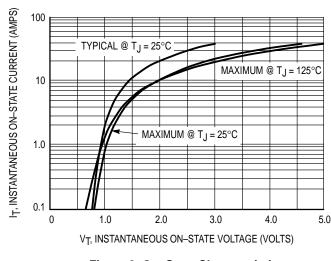
⁽¹⁾ Pulse test: Pulse Width ≤ 2.0 msec, Duty Cycle ≤ 2%.



6.0 P(AV), AVERAGE POWER DISSIPATION (WATTS) dc 180° 5.0 120° 4.0 α = CONDUCTION ANGLE 3.0 2.0 60° α = 30 $^{\circ}$ 1.0 0 1.0 0 2.0 3.0 4.0 I_{T(RMS)}, RMS ON-STATE CURRENT (AMPS)

Figure 1. RMS Current Derating

Figure 2. On-State Power Dissipation



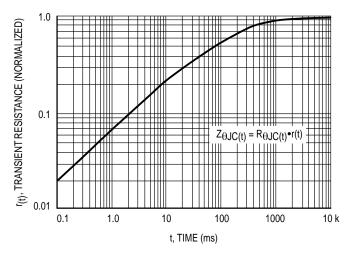
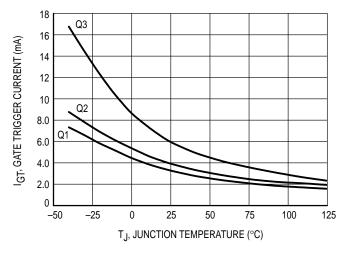


Figure 3. On-State Characteristics

Figure 4. Transient Thermal Response



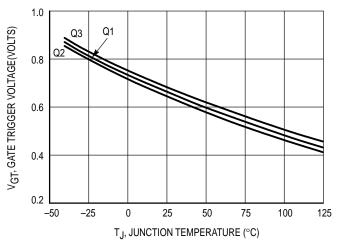


Figure 5. Typical Gate Trigger Current versus
Junction Temperature

Figure 6. Typical Gate Trigger Voltage versus
Junction Temperature

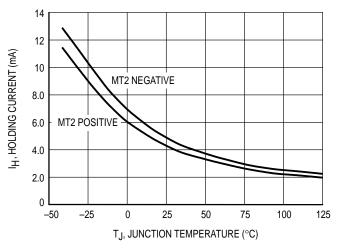


Figure 7. Typical Holding Current versus Junction Temperature

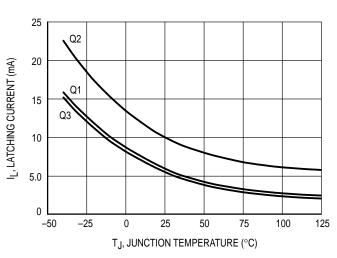


Figure 8. Typical Latching Current versus
Junction Temperature

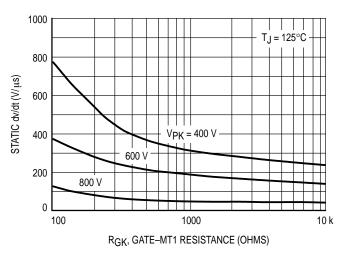


Figure 9. Exponential Static dv/dt versus Gate-MT1 Resistance, MT2(+)

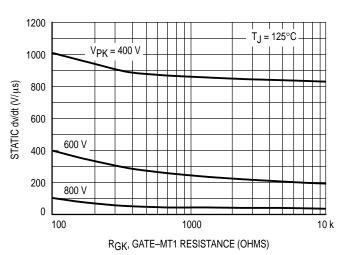


Figure 10. Exponential Static dv/dt versus Gate–MT1 Resistance, MT2(–)

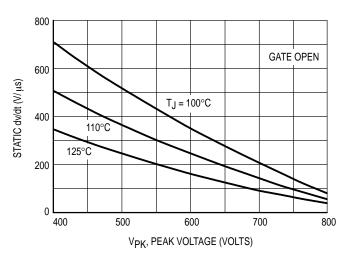


Figure 11. Exponential Static dv/dt versus Peak Voltage, MT2(+)

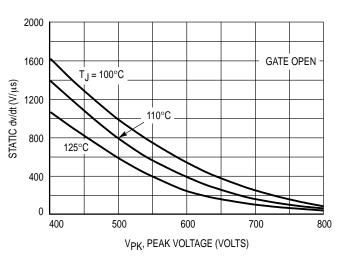
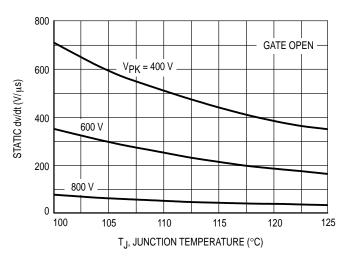


Figure 12. Exponential Static dv/dt versus Peak Voltage, MT2(-)



1600 GATE OPEN 1400 V_{PK} = 400 V 1200 STATIC dv/dt (V/µs) 1000 800 600 V 600 400 200 800 V 0 100 105 110 115 120 125 T_J, JUNCTION TEMPERATURE (°C)

Figure 13. Typical Exponential Static dv/dt versus Junction Temperature, MT2(+)

Figure 14. Typical Exponential Static dv/dt versus Junction Temperature, MT2(-)

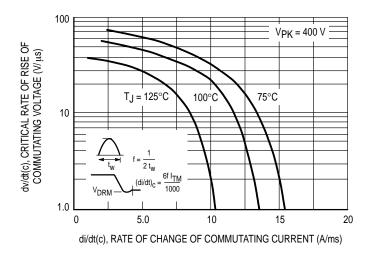
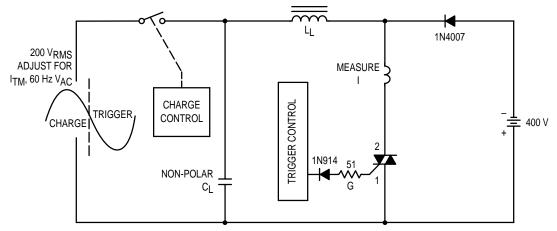


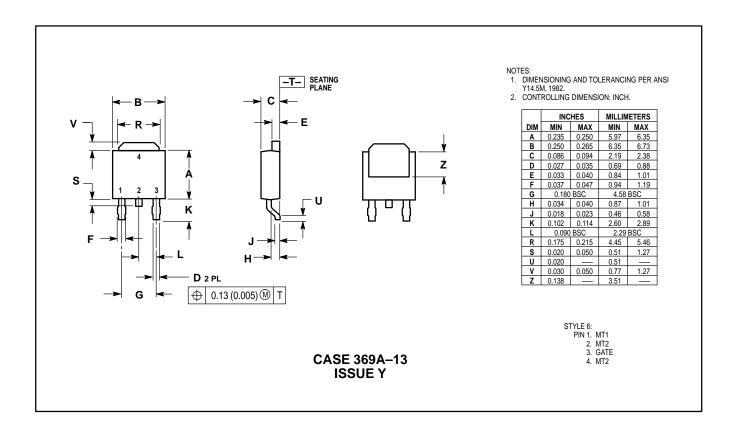
Figure 15. Critical Rate of Rise of Commutating Voltage



Note: Component values are for verification of rated $(dv/dt)_C$. See AN1048 for additional information.

Figure 16. Simplified Test Circuit to Measure the Critical Rate of Rise of Commutating Voltage

PACKAGE DIMENSIONS



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